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FIELD ***Computer Engineering:*** Memory Systems *(DRAM & Non-Volatile Technologies);* Embedded Systems *(Architecture Issues in Real-Time Hardware & Software);* and Technology Innovation *(Entrepreneurship, Audio Systems, & Electric Guitars)*

I. PERSONAL INFORMATION

A. Education

1997 Ph.D. **Computer Science & Engineering** **University of Michigan–Ann Arbor**
Dissertation: *Software-Oriented Memory-Management Design*
Results published in *HPCA (1997), IEEE Computer (1998), IEEE Micro (1998)*

1995 M.S. **Computer Science & Engineering** **University of Michigan–Ann Arbor**
Thesis: *Optimization of Storage Hierarchies*
Results published in *IEEE Transactions on Computers*, vol. 45, no. 10, October 1996

1988 A.B. **Mathematics** *(cum laude)* **Harvard University**
Senior Project: *A Radio Study of the Galactic Center*
Results published in *Interstellar Matter*, Gordon & Breach NY, 1987
Starting PK on 1987 Ivy League Championship football team

B. Professional Experience

2012– **Visiting Professor**, Università degli Studi di Siena, Siena Italy

2011– **Professor**, Department of Electrical & Computer Engineering, University of Maryland, College Park MD

2007–2010 **Director of Computer Engineering**, Department of Electrical & Computer Engineering, University of Maryland, College Park MD

2006– **Founder & CEO**, Coil LLC (doing business as *Coil Guitars*), College Park MD

2006 Named **Keystone Professor**, University of Maryland's Clark School of Engineering

2003–2011 **Associate Professor**, Department of Electrical & Computer Engineering, University of Maryland, College Park MD

1997–2003 **Assistant Professor**, Department of Electrical & Computer Engineering, University of Maryland, College Park MD

1992–1997 **Graduate Student Research Assistant**, University of Michigan, Ann Arbor MI

1991–1992 **System Architect/Chief Engineer**, Priority Call Management, Wilmington MA

1989–1991 **Software Engineer**, Boston Technology, Cambridge MA

1988–1989 **Mathematics Teacher**, Thayer Academy, Braintree MA

II. RESEARCH, SCHOLARLY, AND CREATIVE ACTIVITIES

A. Contracts and Grants

Sandia National Laboratories
E-VERIFY: High Performance Memory Systems Design and Optimization; 2/2012–2/2013; $150,000. PI.

Defense Advanced Research Projects Agency
X-caliber Ubiquitous High Performance Computing (UHPC) Proposal; 10/2010–9/2014; $25,800,000. Academic Subcontractor, on team including Sandia National Laboratories (Lead Institution), FTL Systems, Micron Technologies, LexisNexis Special Services, Indiana Integrated Circuits LLC, Georgia Institute of Technology, Louisiana State University, North Carolina State University, Stanford University, University of Illinois, University of Notre Dame, and University of Southern California.

Department of Energy Office of Science
Data Movement Dominates: Advanced Memory Technology to Address the Real Exascale Power Problem; 10/2010–9/2013; $5,100,000. Co-PI, with investigators at Sandia National Laboratories (Lead Institution), Lawrence Berkeley National Laboratory, Micron Technologies, and Columbia University.

Intel Corporation
Novel Applications of Persistent Memory; 10/2010–9/2013; $440,000. PI.

Sandia National Laboratories
Non-Volatile Memory Systems; 10/2010– 9/2013; $200,000. PI.

Maryland Industrial Partnerships
Novel Signal-Processing Prototypes II; 1/2010–12/2010; $135,000. PI.

Intel Corporation
Memory Hierarchy Architecture Research; 11/2009 [Foundation gift]; $120,000. PI.

Cypress Semiconductor Corporation
Memory-System Modeling; 11/2009–7/2010; $200,000. PI.

Maryland Industrial Partnerships
Novel Signal-Processing Prototypes; 1/2009–12/2009; $135,000. PI.

Department of Defense—Maryland Procurement Office
Next-Generation DRAM-System Architectures and Optimizations; 11/2008–ongoing; $100,000 per year. PI.

Sandia National Laboratories
High Performance Memory-Systems Design and Optimization; 6/2008–12/2010; $255,000. PI.

National Institute of Standards and Technology
Integration Methodologies and Full System Verification for Heterogeneous Systems on Chip; 1/2007–1/2009; $150,000. PI.

Office of the Secretary of Defense
Focused Logistics Transformation and Sense & Respond Support; 9/2005–12/2007; $40,000 per year (my portion). Associated Researcher.

National Science Foundation, MRI Award

MRI: Development of Energy-Efficient Embedded Systems for Wireless Sensor Networks; 8/2005–7/2008; $400,000. Co-PI, with Ephremides (PI), Abshire, Barua, Petrov, Qu, Ulukus, and Vishkin. Equipment grant.

Cray Computer Corporation

High-Bandwidth Controller and System Design; 5/2005–11/2005; $60,000. PI.

IBM Corporation, SUR Award

DRAM Device Configuration and Performance Scalability; 2/2005; $25,000 in equipment. PI.

National Institute of Standards and Technology

System-on-Chip Integration of Microcontroller with Gas Sensor VC; 1/2005–1/2007; $140,000. PI.

Cray Computer Corporation

DDR3 Memory-System Configuration Sensitivity; 4/2004–9/2004; $50,000. PI.

National Institute of Standards and Technology

Embedded Sensor System-on-Chip Microcontroller Core and System Architecture Design; 8/2003–5/2004; $30,000. PI.

National Science Foundation, ITR Award

ITR: Parallel Random-Access Model (PRAM)-On-Chip; 9/2003–9/2008; $750,000. Co-PI, with Vishkin (PI), Barua, Franklin, and Qu.

Department of Defense—Maryland Procurement Office

Joint Program for Advanced Electronic Materials; 6/2003–5/2006; $2,400,000. With Lee (PI), Goldsman, and Yang.

Air Force Office of Scientific Research, MURI Award

Basic Studies of the Effect of Microwave Pulses on Electronics; 5/2001–4/2006; $3,300,000. Co-PI, with Granatstein (PI), Anlage, Antonsen, Baker, Carmel, Goldsman, Iliadis, Melngailis, O'Shea, Ott, Ramahi, and Rodgers.

National Science Foundation

Hardware-Software Co-Design of Real-Time Operating Systems and Embedded Microprocessors; 3/2001–3/2005; $1,400,000. PI, with Stewart (subcontractor).

National Science Foundation, CAREER Award

Architecture Issues in DRAM Devices and Systems; 1/2000–1/2004; $230,000. PI.

Compaq Computer Corporation

Evaluation of EV6 with Contemporary DRAM Architectures; 8/1999; $40,000 in equipment. PI.

IBM Corporation

The Study of Design Parameters for DDR DRAM and DDRII DRAM; 11/1999–1/2003; joint study agreement with access to IBM proprietary mainframe memory traces. PI.

National Science Foundation

Hardware-Software Co-Design of an Experimental Real-Time Operating System and a Microcontroller Architecture; 9/1998–9/2000; $280,000. Co-PI, with Stewart (PI).

UNIVERSITY OF MARYLAND INTERNAL:

UMD Minta Martin Aeronautical Research Fund
Microarchitecture Support for Real-Time Embedded Systems; 5/1998–10/1999; $35,000.

UMD General Research Board Summer Research
A Better Simulation Environment for Computer Architecture; 6/1998–9/1998; $6,000.

Note: *In the following sections on publications, lead author is first; student advisees are in* ***bold****; paper acceptance rate is given where known; number of citations is given only for works whose citation count is notable (e.g., double digits). Citation counts come from Google Scholar and include self-citations.*

Total number of citations > 2000; h-index of citations = 24 *(24+ works have 24+ cites each);*
g-index of citations = 45 *(45 is largest* ***i*** *for which* ***i*** *≤ sqrt[total citations for* ***i*** *most cited works]);*
i100-index of citations = 4 *(the number of publications with at least 100 citations);*
mean citations per work = 31; mean citations per cited work = 33; *means exclude Edited Work.*

B. BOOKS

1. B. Jacob, with contributions by **S. Srinivasan** and **D. T. Wang**. The Memory System (You Can't Avoid It; You Can't Ignore It; You Can't Fake It). ISBN 978-1598295870. Morgan & Claypool Publishers: San Rafael CA, 2009.

2. B. Jacob, S. Ng, and **D. Wang**, with contributions by **S. Rodriguez**. Memory Systems: Cache, DRAM, Disk. ISBN 978-0123797513. Morgan Kaufmann: San Francisco CA, 2007.

   Citations: 163

   ➡ ~500,000 words, 950 pages. An authored work, not an edited work.

C. PAPERS IN HIGHLY COMPETITIVE CONFERENCE PROCEEDINGS

In computer engineering, journals take two or more years from submission to print. In a field that changes as rapidly as this, such a delay means that, by publication, the core idea in a paper can become obsolete or at least far less interesting than at the time of submission. Such a delay ensures that few, if any, researchers will read the paper when it finally emerges in print. For this reason, in computer systems, certain conferences have become preferred over all journals as avenues for the dissemination of researchers' best ideas—for example, the unquestionably top forums in processor & system design (one subset of computer engineering) are the ISCA, ASPLOS, MICRO, and HPCA conferences. The analogous forums in embedded systems are CASES, CODES+ISSS, ISLPED, and DAC.

It is to these top conferences, and not to journals, that researchers in this field send their very best work. To ensure high quality, symposia in computer engineering, from workshops to the most competitive of conferences, are archival, require the submission of full papers for review (6000–9000 word papers, not abstracts or extended abstracts), and have extremely competitive acceptance rates, often in the range of 15–20%.

1. **E. Cooper-Balis**, **P. Rosenfeld**, and B. Jacob. "Buffer On Board memory systems." In *Proc. 39th International Symposium on Computer Architecture (**ISCA** 2012)*, pp. 392–403. Portland OR, June 2012.

   Acceptance: 47/262 (18%)

2. **C. Dirik** and B. Jacob. "The performance of PC Solid-State Disks (SSDs) as a function of bandwidth, concurrency, device architecture, and system organization." In *Proc. 36th International Symposium on Computer Architecture (**ISCA** 2009)*, pp. 279–289. Austin TX, June 2009.

   Acceptance: 43/210 (20%) — Citations: 73

3. **B. Ganesh**, **A. Jaleel**, **D. Wang**, and B. Jacob. "Fully-Buffered DIMM memory architectures: Understanding mechanisms, overheads and scaling." In *Proc. 13th International Symposium on High Performance Computer Architecture (**HPCA** 2007)*, pp. 109–120. Phoenix AZ, February 2007.

   Acceptance: 28/174 (16%) — Citations: 37

4. **A. Varma**, Y. Afridi, A. Akturk, P. Klein, A. Hefner, and B. Jacob. "Modeling heterogeneous SoCs with SystemC: A digital/MEMS case study." In *Proc. International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (**CASES** 2006)*, pp. 54–64. Seoul Korea, October 2006.

   Acceptance: 41/100 (41%)

5. **S. V. Rodriguez** and B. Jacob. "Energy/power breakdown of pipelined nanometer caches (90nm/65nm/45nm/32nm)." In *Proc. International Symposium on Low Power Electronics and Design (**ISLPED** 2006)*, pp. 25–30. Tegernsee Germany, October 2006.

   Acceptance: 56/214 (26%) — Citations: 36

6. **A. Jaleel**, M. Mattina, and B. Jacob. "Last-level cache (LLC) performance of data-mining workloads on a CMP—A case study of parallel bioinformatics workloads." In *Proc. 12th IEEE International Symposium on High Performance Computer Architecture (**HPCA** 2006)*, pp. 88–98. Austin TX, February 2006.

   Acceptance: 26/172 (15%) — Citations: 79

7. K. Albayraktaroglu, **A. Jaleel**, X. Wu, M. Franklin, B Jacob, C. Tseng, and D. Yeung. "BioBench: A benchmark suite of bioinformatics applications." In *Proc. 2005 IEEE International Symposium on Performance Analysis of Systems and Software (**ISPASS** 2005)*, pp. 2–9. Austin TX, March 2005.

   Acceptance: 27/92 (29%) — Citations: 76

8. **A. Jaleel** and B. Jacob. "Using virtual load/store queues (VLSQs) to reduce the negative effects of reordered memory instructions." In *Proc. 11th IEEE International Symposium on High Performance Computer Architecture (**HPCA** 2005)*, pp. 191–200. San Francisco CA, February 2005.

   Acceptance: 28/181 (15%)

   ➡ Aamer Jaleel won the *Best Paper Presentation* award for his talk presenting this paper (*International Symposium on High Performance Computer Architecture*, February 2005).

9. **B. Iyer**, **S. Srinivasan**, and B. Jacob. "Extended Split-Issue: Enabling flexibility in the hardware implementation of NUAL VLIW DSPs." In *Proc. 31st Annual ACM/IEEE International Symposium on Computer Architecture (**ISCA** 2004)*, pp. 364–375. München Germany, June 2004.

   Acceptance: 31/217 (14%) — Citations: 11

10. **A. Varma**, **B. Ganesh**, M. Sen, S. R. Choudhary, L. Srinivasan, and B. Jacob. "A control-theoretic approach to dynamic voltage scheduling." In *Proc. International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (**CASES** 2003)*, pp. 255–266. San Jose CA, October 2003.

    Acceptance: 31/162 (19%) — Citations: 68

11. **P. Kohout**, **B. Ganesh**, and B. Jacob. "Hardware support for real-time operating systems." In Proc. *First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (**CODES+ISSS** 2003)*, pp. 45–51. Newport Beach CA, October 2003.

    Acceptance: 30/143 (20%) — Citations: 84

12. **K. Baynes**, **C. Collins**, **E. Fiterman**, **B. Ganesh**, **P. Kohout**, **C. Smit**, **T. Zhang**, and B. Jacob. "The performance and energy consumption of three embedded real-time operating systems." In *Proc. International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (**CASES** 2001)*, pp. 203–210. Atlanta GA, November 2001.

    Acceptance: 28/80 (35%) — Citations: 37

13. **S. Srinivasan**, **V. Cuppu**, and B. Jacob. "Transparent data-memory organizations for digital signal processors." In *Proc. International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (**CASES** 2001)*, pp. 44–48. Atlanta GA, November 2001.

    Acceptance: 28/80 (35%)

14. **V. Cuppu** and B. Jacob. "Concurrency, latency, or system overhead: Which has the largest impact on uniprocessor DRAM-system performance?" In *Proc. 28th Annual ACM/IEEE International Symposium on Computer Architecture (**ISCA** 2001)*, pp. 62–71. Göteborg, Sweden, June 2001.

    Acceptance: 24/163 (15%) — Citations: 69

15. **V. Cuppu**, B. Jacob, B. Davis, and T. Mudge. "A performance comparison of contemporary DRAM architectures." In *Proc. 26th Annual ACM/IEEE International Symposium on Computer Architecture (**ISCA** 1999)*, pp. 222–233. Atlanta GA, May 1999.

    Acceptance: 26/135 (19%) — Citations: 176

16. B. Jacob. "Hardware/software architectures for real-time caching." In *Proc. International Conference on Compiler and Architecture Support for Embedded Systems (**CASES** 1999)*, pp. 135–138. Washington DC, October 1999.

17. D. Stewart and B. Jacob. "Hardware/software co-design of I/O interfacing hardware and real-time device drivers for embedded systems." In *Proc. International Conference on Compiler and Architecture Support for Embedded Systems (**CASES** 1999)*, pp. 115–119. Washington DC, October 1999.

18. B. Jacob. "Software-managed caches: Architectural support for real-time embedded systems." In *Proc. International Conference on Compiler and Architecture Support for Embedded Systems (**CASES** 1998)*. Washington DC, December 1998.

19. B. Jacob and T. Mudge. "A look at several memory-management units, TLB-refill mechanisms, and page table organizations." In *Proc. Eighth ACM/IEEE International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS** 1998)*, pp. 295–306. San Jose CA, October 1998.

    Acceptance: 28/123 (23%) — Citations: 69

20. B. Jacob and T. Mudge. "Software-managed address translation." In *Proc. Third IEEE International Symposium on High Performance Computer Architecture (**HPCA** 1997)*, pp. 156–167. San Antonio TX, February 1997.

    Acceptance: 30/150 (20%) — Citations: 57

D. Articles in Refereed Journals

21. A. Rodrigues, K. Hemmert, B. Barrett, C. Kersey, R. Oldfield, M. Weston, R. Risen, J. Cook, **P. Rosenfeld**, **E. Cooper-Balls**, and B. Jacob. "The Structural Simulation Toolkit." *ACM SIGMETRICS Performance Evaluation Review*, vol. 38, no. 4, pp. 37–42. March 2011.

    Citations: 19

22. **E. Cooper-Balis** and B. Jacob. "Fine grained activation for power reduction in DRAM." *IEEE Micro*, vol. 30, no. 3, pp. 34-47. May/June 2010.

    Citations: 11

23. **A. Varma**, E. Debes, I. Kozintsev, P. Klein, and B. Jacob. "Accurate and fast system-level power modeling: An XScale-based case study." *ACM Transactions on Embedded Computing Systems*, vol. 7, no. 3, pp. 25:1–25:20. April 2008.

    Citations: *see September 2007 printing of article, below*

    ➡ Identical to September 2007 article of same title; reason for reprinting unknown.

24. **A. Varma**, B. Jacob, E. Debes, I. Kozintsev, and P. Klein. "Accurate and fast system-level power modeling: An XScale-based case study." *ACM Transactions on Embedded Computing Systems*, vol. 6, no. 4, pp. 26:1–26:20. September 2007. (special issue on best papers from LCTES'05)

    Citations: 18

25. **A. Jaleel** and B. Jacob. "In-line interrupt handling and lock-up free translation lookaside buffers (TLBs)." *IEEE Transactions on Computers*, vol. 55, no. 5, pp. 559–574. May 2006.

    Citations: 14

26. **H. Wang**, **S. V. Rodriguez**, **C. Dirik**, and B. Jacob. "Electromagnetic interference and digital circuits: An initial study of clock networks." *Electromagnetics*, vol. 26, no. 1, pp. 73–86. January 2006. (special issue on RF effects on digital systems)

    Citations: 12

27. **D. Wang**, **B. Ganesh**, **N. Tuaycharoen**, **K. Baynes**, **A. Jaleel**, and B. Jacob. "DRAMsim: A memory-system simulator." *SIGARCH Computer Architecture News*, vol. 33, no. 4, pp. 100–107. September 2005.

    Citations: 148

28. M. Afridi, A. Hefner, D. Berning, C. Ellenwood, **A. Varma**, B. Jacob, S. Semancik. "MEMS-based embedded sensor virtual components for system-on-a-chip (SoC)." *Solid-State Electronics*, vol. 48, no. 10/11, pp. 1777–1781. October/November 2004.

    Citations: 40

29. **K. Baynes**, **C. Collins**, **E. Fiterman**, **B. Ganesh**, **C. Smit**, **T. Zhang**, and B. Jacob. "The performance and energy consumption of embedded real-time operating systems." *IEEE Transactions on Computers*, vol. 52, no. 11, pp. 1454–1469. November 2003.

    Citations: 56

30. B. Jacob. "A case for studying DRAM issues at the system level." *IEEE Micro*, vol. 23, no. 4, pp. 44–56. July/August 2003.

    Citations: 23

31. **V. Cuppu**, B. Jacob, B. Davis, and T. Mudge. "High performance DRAMs in workstation environments." *IEEE Transactions on Computers*, vol. 50, no. 11, pp. 1133–1153. November 2001. (special issue on high-performance memory systems)

    Citations: 40

32. B. Jacob and T. Mudge. "Uniprocessor virtual memory without TLBs." *IEEE Transactions on Computers*, vol. 50, no. 5, pp. 482–499. May 2001.

    Citations: 22

33. B. Jacob and T. Mudge. "Virtual memory in contemporary microprocessors." *IEEE Micro*, vol. 18, no. 4, pp. 60–75. July/August 1998.

    Citations: 64

34. B. Jacob and T. Mudge. "Virtual memory: Issues of implementation." *IEEE Computer*, vol. 31, no. 6, pp. 33–43. June 1998.

    Citations: 68

    ➡ Listed as an editor's must-read pick in the "Literature Watch" column of *Microprocessor Report*, vol. 12, no. 12, p. 24. September 14, 1998.

35. B. Jacob, P. Chen, S. Silverman, and T. Mudge. "A comment on 'An analytical model for designing memory hierarchies.'" *IEEE Transactions on Computers*, vol. 46, no. 10, p. 1151. October 1997.

36. B. Jacob. "Algorithmic composition as a model of creativity." *Organised Sound*, Cambridge University Press, vol. 1, no. 3, pp. 157–165. December 1996.

    Citations: 53

37. B. Jacob, P. Chen, S. Silverman, and T. Mudge. "An analytical model for designing storage hierarchies." *IEEE Transactions on Computers*, vol. 45, no. 10, pp. 1180–1194. October 1996.

    Citations: 72

E. Editorial Work

38. B. Jacob and S. Bhattacharyya, Editors. Embedded Systems: The Memory Resource. Special (and inaugural) issue of *ACM Transactions on Embedded Computing Systems*, vol. 1, no. 1, September 2002.

F. Chapters in Books

39. B. Jacob. "Reward: How to Foster a Technology-Innovation Culture within a Large Organization (What You Can Learn from Startup Companies)." In The Handbook of Technology Management, pp. 1:964–1:977. H. Bidgoli, Editor. John Wiley & Sons: Hoboken NJ, 2009.
40. B. Jacob. "Virtual Memory." In Computer Sciences. R. Flynn, Editor. Macmillan Reference USA: Farmington Hills MI, 2002.
41. B. Jacob. "Virtual Memory Systems and TLB Structures." In The Computer Engineering Handbook, pp. 5:55–5:65. V. Oklobdzija, Editor. CRC Press: Boca Raton FL, 2002.
    - ➡ In February, 2003, The Computer Engineering Handbook was honored as an Outstanding Academic Title for 2002 by *Choice Magazine*, a publication of the American Library Association.
42. B. Jacob, J. Szczepanski, and P. Ho. "SiO J=1–0 Emission Near the Galactic Center: Tidal Stripping and Shocks?" In Interstellar Matter. Gordon and Breach: New York NY, 1987.

G. Papers in Refereed Conferences

43. **S. Srinivasan**, L. Zhao, **B. Ganesh**, B. Jacob, M. Espig, and R. Iyer. "CMP memory modeling: How much does accuracy matter?" In *Proc. Fifth Annual Workshop on Modeling, Benchmarking and Simulation (MoBS)*, pp. 24–33. Austin TX, June 2009.
44. **A. Jaleel**, R. S. Cohn, C.-K. Luk, and B. Jacob. "CMP$im: A Pin-based on-the-fly multi-core cache simulator." In *Proc. Fourth Annual Workshop on Modeling, Benchmarking and Simulation (MoBS)*, pp. 28–36. Beijing China, June 2008.

    Citations: 66
45. **A. Varma**, E. Debes, I. Kozintsev, and B. Jacob. "Instruction-level power dissipation in the Intel XScale embedded microprocessor." In *Proc. SPIE's 17th Annual Symposium on Electronic Imaging Science & Technology*, vol. 5683, pp. 1–8. San Jose CA, January 2005.

    Citations: 19
46. **H. Wang**, **S. V. Rodriguez**, **C. Dirik**, **A. Gole**, **V. Chan**, and B. Jacob. "TERPS: The Embedded Reliable Processing System." A finalist in the University LSI Design Contest. *Asia and South Pacific Design Automation Conference 2005 (ASP-DAC 2005)*. Shanghai China, January 2005.
47. J. Teller, C. Silio, and B. Jacob. "Performance characteristics of MAUI: an intelligent memory system architecture." In *Proc. Workshop on Memory System Performance (MSP 2005)*, pp. 44–53. Chicago IL, June 2005.

48. **H. Wang**, **C. Dirik**, **S. V. Rodriguez**, **A. V. Gole** and B. Jacob. "Radio frequency effects on the clock networks of digital circuits." In *Proc. IEEE International Symposium on Electromagnetic Compatibility (EMC 2004)*. Santa Clara CA, August 2004.

    Citations: 10

49. M. Afridi, A. Hefner, D. Berning, C. Ellenwood, **A. Varma**, B. Jacob, S. Semancik. "MEMS-based embedded sensor virtual components for SoC." In *Proc. International Semiconductor Device Research Symposium (ISDRS 2003)*. Washington DC, December 2003.

50. **A. Jaleel** and B. Jacob. "In-line interrupt handling for software-managed TLBs." In *Proc. 19th IEEE International Conference on Computer Design (ICCD 2001)*, pp 62–67. Austin TX, September 2001.

    Acceptance: 61/181 (34%) — Citations: 14

51. **A. Jaleel** and B. Jacob. "Improving the precise interrupt mechanism of software-managed TLB miss handlers." In *High Performance Computing, Lecture Notes in Computer Science*, Vol. 2228, pp. 282–293. B. Monien, V. Prasanna, and S. Vajapeyam, Editors. Springer Publishing: Berlin, Germany, 2001.

52. B. Davis, T. Mudge, and B. Jacob. "The new DRAM interfaces: SDRAM, RDRAM and variants." In *High Performance Computing, Lecture Notes in Computer Science*, Vol. 1940, pp. 26–31. M. Valero, K. Joe, M. Kitsuregawa, and H. Tanaka, Editors. Springer Publishing: Tokyo, Japan, 2000.

    Citations: 10

53. B. Davis, T. Mudge, **V. Cuppu**, and B. Jacob. "DDR2 and low-latency variants." In *Proc. Workshop on Solving the Memory Wall Problem*, pp. 15–29. Vancouver, British Columbia, June 2000.

    Acceptance: 13/40 (33%) — Citations: 26

54. B. Jacob. "Cache design for embedded real-time systems." In *Proc. Embedded Systems Conference*, Summer. Danvers MA, June 1999. CD-ROM proceedings.

    Citations: 16

55. B. Jacob. "Service Discovery: Access to local resources in a nomadic environment." *OOPSLA'96 Workshop on Object Replication and Mobile Computing*. San Jose CA, October 1996. The original extended abstract submitted to the conference was entitled "Support for nomadism in a global environment," which is the title given on some websites.

56. B. Jacob and T. Mudge. "The trading function in action." In *Proc. 1996 ACM SIGOPS European Workshop*, pp. 241–247. Connemara, Ireland, September 1996.

57. B. Jacob. "Composing with genetic algorithms." In *Proc. 1995 International Computer Music Conference (ICMC 1995)*, pp. 452–455. Banff, Alberta, September 1995.

    Acceptance: 190/240 (79%) — Citations: 103

58. B. Jacob. "The use of distributed objects and dynamic interfaces in a wide-area transaction environment." *SIGCOMM '95 Workshop on Middleware*. Cambridge MA, August 1995.

H. Technical Reports & White Papers

59. B. Jacob. "On supporting a high-tech cottage industry ... an open letter to the engineering-education community." December 2007.

60. **A. Jaleel**, R. S. Cohn, C-K. Luk, and B. Jacob. "CMP$im: A binary instrumentation approach to modeling memory behavior of workloads on CMPs." Tech. Rep. UMD-SCA-2006-01, University of Maryland Systems & Computer Architecture Group. June 2006.

    Citations: 11

61. B. Jacob and S. Bhattacharyya. "Real-time memory management: Compile-time techniques and run-time mechanisms that enable the use of caches in real-time systems." Tech. Rep. UMIACS-TR-2000-60, University of Maryland Institute for Advanced Computer Studies (UMIACS). September 2000.

62. **C. Collins**, **E. Fiterman**, **T. Zhang**, and B. Jacob. "SimBed: Accurate microarchitecture-level simulation of embedded real-time operating systems." Tech. Rep. UMD-SCA-2000-1, University of Maryland Systems & Computer Architecture Group. April 2000.

63. **V. Cuppu** and B. Jacob. "Organizational design trade-offs at the DRAM, memory bus, and memory controller level: Initial results." Tech. Rep. UMD-SCA-1999-2, University of Maryland Systems & Computer Architecture Group. November 1999.

    Citations: 11

64. E. Berkovich, J. Nuzman, M. Franklin, B. Jacob, and U. Vishkin. "XMT-M: A scalable decentralized processor." Tech. Rep. UMIACS-TR-99-55. University of Maryland Institute for Advanced Computer Studies (UMIACS). October 1999.

65. B. Jacob. "Segmented addressing solves the virtual cache synonym problem." Tech. Rep. UMD-SCA-1997-1, University of Maryland Systems & Computer Architecture Group. December 1997.

66. B. Jacob. *Software-Oriented Memory-Management Design*. PhD thesis, The University of Michigan. July 1997.

67. B. Jacob. "Notes on calculating computer performance." Tech. Rep. CSE-TR-231-95, University of Michigan. March 1995.

68. B. Jacob. "Optimization of mass storage hierarchies." M.S. thesis, Tech. Rep. CSE-TR-228-95, The University of Michigan. May 1994.

I. Invited Presentations

1. "Big Memories." Keynote, Session on Large Memory Systems & Challenges at *International Supercomputing Conference*, Hamburg Germany, Spring 2012.

2. "Data Access, Data Movement, Data Integrity." Spring 2012.

    ➡ One of roughly a dozen members of academia, industry, and the national laboratories who were asked to brief Secretary Chu on the status of supercomputing today and what is required to achieve exascale performance in the near future.

3. "Research and Development in Electrical & Computer Engineering." Invited talk, *Career Day at Baltimore Polytechnic Institute*, Baltimore MD, Spring 2010.

4. "Memory Systems: Then, Now, and To Come." Keynote, Session on Memory Systems at *International Supercomputing Conference*, Hamburg Germany, Spring 2010.
5. "Trends in Memory Systems." *Sun-DARPA UNIC Architecture Workshop*, Menlo Park CA, Winter 2010.
6. "Wealth, Innovation, Design, & Entrepreneurship." *University of Maryland Department of Electrical & Computer Engineering Advisory Board,* Fall 2009.
7. "Innovation & Design ... and Modern Engineering Entrepreneurship." *University of Maryland Clark School Board of Visitors*, Fall 2009.
8. "High-Tech Design as Modern Engineering Entrepreneurship." U. Maryland *ECEGSA Seminar Series*, Fall 2009.
9. "Embedded Systems, Memory Systems, and Embedded Memory Systems." *ACACES 2009 Fifth International Summer School on Advanced Computer Architecture and Compilation for Embedded Systems*, Terrassa Spain, Summer 2009.
10. "R&D in Electrical & Computer Engineering." *National Student Leadership Conference*, Summer 2009.
11. "The Memory System and You: A Love/Hate Relationship." *SOS-13 Workshop on Distributed Supercomputing*, Hilton Head SC, Spring 2009.
12. "R&D in Electrical & Computer Engineering." *National Student Leadership Conference*, Summer 2008.
13. "Engineering Entrepreneurship: Towards a High-Tech Cottage Industry." *Inventis Lecture Series on Professional Concepts in Engineering*, University of Maryland, Spring 2008.
14. "Memory Systems." Briefing at *National Academies CSTB Workshop on Trends in Computing Performance*, Mountain View CA, Fall 2007.

    ➡ One of ten people across all areas of computing (including sub-disciplines of Storage, Power, Programming, and Applications) invited to brief a National Academies committee on the state of affairs in our various sub-disciplines. Briefers were asked to inform the committee on technical issues and present/future trends that can hinder or aid the continued growth of computer performance. More info can be found at http://www7.nationalacademies.org/CSTB/project_computing-performance.html.
15. "Design as Modern Engineering Entrepreneurship." Invited lecture for *UNIV 100, The Student and the University*, Fall 2007.
16. "Embedded and Non-Classical Systems." *Dialogue with the Dean* lecture series, University of Maryland College of Engineering, Spring 2006.
17. "A Holistic Approach to DRAM (and Systems)." North Carolina State University, Raleigh NC, Spring 2006.
18. "A Holistic Approach to DRAM-System Design." IBM T.J. Watson Research Center, Yorktown Heights NY, Winter 2004.
19. "A Bad Talk, A Good Talk, A Bad Talk, A Good Talk, Some Thoughts (or: How Not To Suck)." First presented at U. Maryland *ECEGSA Seminar Series*, Spring 2004.

20. "Research Issues in Embedded Systems." *Dialogue with the Dean* lecture series, University of Maryland College of Engineering, Fall 2003.
21. "Embedded Systems at Maryland." University of Maryland College of Engineering, Department of Electrical Engineering, Department of Computer Science, Institute for Advanced Computer Studies, and Institute for Systems Research Research Review Day, Spring 2003.
22. "How To Do Research (Well)." First presented at U. Maryland *ECEGSA Seminar Series*, Spring 2003.
23. "Computers and Memory Systems." *Dialogue with the Dean* lecture series, University of Maryland College of Engineering, Fall 2001.
24. "Career Paths in Computer Engineering, or So What Are You Going To Do With Your Life?" *University of Maryland IEEE Student-Professional Awareness Conference (S-PAC)*, Spring 2001.
25. "How Not to Configure Your DRAM System." Compaq Systems Research Group, Marlborough MA, Fall 2000.
26. "High-Performance DRAM Systems." Compaq Alpha Group, Shrewsbury MA, Fall 2000.
27. "Contemporary DRAM Architectures and Beyond." Compaq Systems Research Center, Palo Alto CA, Fall 1999.
28. "Cache Design for Embedded Real-Time Systems." *Embedded Systems Conference*, Danvers MA, Spring 1999.
29. "DRAM Memory Systems." IBM T.J. Watson Research Center, Yorktown Heights NY, Spring 1999.
30. "The Top 10 Lessons I Learned as a Grad Student." University of Maryland Electrical & Computer Engineering Department, Fall 1998.

    ➡ This is a talk I gave for the first time Fall 1998; since then, I have been asked to give it roughly twice a year by various organizations on campus.
31. "Software-Managed Memory Systems." University of Wisconsin Electrical & Computer Engineering Department, Madison WI, Spring 1998.
32. "The IA-64 Architecture." University of Maryland IEEE Chapter, Fall 1997.

J. Conference Presentations

33. "Energy/Power Breakdown of Pipelined Nanometer Caches (90nm/65nm/45nm/32nm)." Presented at The International Symposium on Low Power Electronics and Design (ISLPED 2006), Tegernsee Germany, October 2006.
34. "Concurrency, Latency, or System Overhead: Which Has the Largest Impact on Uniprocessor DRAM-System Performance?" Presented at The 28th International Symposium on Computer Architecture (ISCA-28), Göteborg Sweden, June 2001.
35. "Hardware/Software Architectures for Real-Time Caching." Presented at CASES'99: The Second International Workshop on Compiler and Architecture Support for Embedded Systems, Washington DC, December 1999.

36. "A Performance Comparison of Contemporary DRAM Architectures." Presented at The 26th Annual ACM/IEEE International Symposium on Computer Architecture (ISCA-26), Atlanta GA, May 1999.

37. "Software-Managed Caches: Architectural Support for Real-Time Embedded Systems." Presented at CASES'98: IEEE Workshop on Compiler and Architecture Support for Embedded Systems, Washington DC, December 1998.

38. "A Look at Several Memory Management Units, TLB-Refill Mechanisms, and Page Table Organizations." Presented at The Eighth ACM/IEEE International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-8), San Jose CA, October 1998.

39. "Software-Managed Address Translation." Presented at The Third IEEE International Symposium on High Performance Computer Architecture (HPCA-3), San Antonio TX, February 1997.

40. "Method Invocation in the Face of Anarchy." Presented at The 1996 OOPSLA Workshop on Object Replication and Mobile Computing (ORMC'96), San Jose CA, October 1996.

41. "Composing with Genetic Algorithms." Presented at The 1995 International Computer Music Conference (ICMC'95), Banff Alberta, September 1995.

K. Patents Issued & Pending

1. *System and Method for Performing Multi-Rank Command Scheduling in DDR SDRAM Memory Systems*. US Patent 7,543,102, issued June 2, 2009, filed April 17, 2006, claiming priority to provisional patent filed April 18, 2005. Bruce Jacob and Dave Wang, University of Maryland.

2. *Electronic Guitar Harness Component Connector*. US Patent Application 12/854,166, issuance allowed on December 23, 2010; filed August 10, 2010. Bruce Jacob.

3. *Programmable Switch for Configuring Circuit Topologies*. US Patent Application 12/234,682, filed September 21, 2008. Bruce Jacob.

4. *A Volume-Adjustment Circuit for Equilibrating Pickup Settings*. US Patent Application 12/371,224, filed February 13, 2009. Bruce Jacob.

L. Computational Artifacts

BioBench/BioParallel, developed 2004–2005

A collection of benchmarks, each a different application area within the larger domain of bioinformatics and data mining. BioBench, a suite of workloads collected by students and faculty at the University of Maryland, was released in 2005. The suite expanded in 2006 with the addition of parallel workloads collected by researchers at Intel (distinguished from the original *BioBench* suite as the *BioParallel* suite). Described in the following publications:

K. Albayraktaroglu, **A. Jaleel**, X. Wu, M. Franklin, B Jacob, C. Tseng, and D. Yeung. "BioBench: A benchmark suite of bioinformatics applications." In *Proc. ISPASS 2005*, pp. 2–9. Austin TX, March 2005.

A. Jaleel, M. Mattina, and B. Jacob. "Last-level cache (LLC) performance of data-mining workloads on a CMP—A case study of parallel bioinformatics workloads." In *Proc. HPCA 2006*, pp. 88–98. Austin TX, February 2006.

The benchmark suites have been released to the community and can be found at www.ece.umd.edu/biobench.

DRAMsim, developed 1999–present (ongoing)

A memory-system simulation framework that interacts with popular CPU simulators such as GEMS, MASE, and SimAlpha. It has been developed by my graduate students and represents roughly 25 student-years of development effort. The framework is described in the following publication:

D. Wang, B. Ganesh, N. Tuaycharoen, K. Baynes, A. Jaleel, and B. Jacob. "DRAMsim: A memory-system simulator." *SIGARCH Computer Architecture News*, vol. 33, no. 4, pp. 100–107. September 2005.

The software has been released to the community under the GNU Public License and can be found at www.ece.umd.edu/dramsim.

Variations, developed 1994–1996

A music composition system that uses genetic algorithms to generate and organize complex tonal and microtonal music for orchestral organizations. The software is described in the following publications:

B. Jacob. "Algorithmic composition as a model of creativity." *Organised Sound*, vol. 1, no. 3, pp. 157–165, December 1996.

B. Jacob. "Composing with genetic algorithms." In *Proc. 1995 International Computer Music Conference*, pp. 452–455. Banff, Alberta, September 1995.

High-fidelity audio examples of the system's output (in MP3 format) as well as the software itself can be found at www.ece.umd.edu/~blj/algorithmic_composition.

Telecom Services Architecture, developed 1991–1996

A distributed system of active network objects whose service methods are invoked transparently via a service broker. The software is described in the following publications:

B. Jacob and T. Mudge. "The trading function in action." In *Proc. 1996 ACM SIGOPS European Workshop*, pp. 241–247. Connemara, Ireland, September 1996.

B. Jacob. "The use of distributed objects and dynamic interfaces in a wide-area transaction environment." *SIGCOMM '95 Workshop on Middleware*. Cambridge MA, August 1995.

This architecture was created while starting up the telecommunications company Priority Call Management. The software forms the core technology in Priority Call's product line, and the architecture was still in use as late as 1999.

M. Honors and Awards

University of Maryland "Research Leader" (2012)

Recognized by the University of Maryland's Division of Research as "having made significant contributions to the University of Maryland College Park research program."

University of Maryland "Research Leader" (2010)

Recognized by the University of Maryland's Division of Research as "having made significant contributions to the University of Maryland College Park research program."

Philip Merrill Presidential Scholar Faculty Mentor (2009)

Recognized as the faculty mentor who has made the most impact on the academic achievement of one of the University of Maryland's Philip Merrill Presidential Scholars.

Clark School of Engineering Keystone Professor (2006)

One of six professors named to Keystone: The Clark School Academy of Distinguished Professors.

University of Maryland "Research Leader" (2006)

Recognized by the Office of Research and Graduate Studies for being one of the top 100 researchers in the University of Maryland, as measured by research funding.

University of Maryland "Rainmaker" (2005)

Recognized by the Office of Research and Graduate Studies for being one of the top 100 researchers in the University of Maryland, as measured by research funding.

Best Paper Presentation (HPCA 2005)

My student, Aamer Jaleel, won the Award for Best Paper Presentation for our paper in the *11th Int'l Symposium on High Performance Computer Architecture (HPCA 2005)*, February 2005.

Award for Teaching Excellence (2004)

Recognized by the University of Maryland (campus-wide) for excellence in teaching at the undergraduate level.

University of Maryland "Rainmaker" (2001)

Recognized by the Office of Research and Graduate Studies for being one of the top 100 researchers in the University of Maryland, as measured by research funding.

National Science Foundation CAREER Award (1999)

Project Title: "Architecture Issues in DRAM Devices and Systems."

George Corcoran Memorial Award (1998–9 Academic Year)

"In recognition of teaching and educational leadership at the University of Maryland, College Park campus, effective contribution at the national level, and creative and other scholarly activities related to Electrical and Computer Engineering education."

N. Reviewing Activities

Associate Editor of *IEEE Computer Architecture Letters*, 2007–present

Associate Editor of *ACM Transactions on Embedded Computing Systems*, 2006–2009

Reviewer for papers in the following journals:

IEEE Transactions on Computers
IEEE Transactions on Parallel and Distributed Systems
IEEE Computer
ACM Transactions on Embedded Computing Systems
ACM Transactions on Architecture and Code Optimization
ACM Computing Surveys
IBM Journal of Research and Development
The Computer Journal

Reviewer for papers in the following annual meetings:

ACM/IEEE International Symposium on Computer Architecture (ISCA)

ACM/IEEE International Symposium on Microarchitecture (MICRO)
ACM International Conference on Supercomputing (ICS)
IEEE International Symposium on High-Performance Computer Architecture (HPCA)
IEEE International Symposium on High-Assurance Systems Engineering (HASE)
IEEE International Conference on Computer Design (ICCD)
Int'l Conf. on Compilers, Architectures, and Synthesis for Embedded Systems (CASES)
Workshop on Computer Architecture Education (WCAE)

O. Professional Memberships

1993–	Member, ACM
1994–	Member, IEEE
1993–1998	Member, USENIX
1999–	USENIX Campus Liaison at University of Maryland

III. TEACHING AND ADVISING

A. Course Instruction

Teaching evaluation scores are often in the top half dozen scores in the department (out of roughly 70 faculty); they have been the highest-ranking score in the department on at least three occasions.

Semester	Course No.	Course Title	No. of Students	Teach. Eval. Total Grade	Dept/Coll Avg.
Fall 1997	ENEE 350H	*Computer Organization (Honors)*	12	3.81	3.36
Spring 1998	ENEE 759M	*Advanced Topics in Microarchitecture*	15	3.71	3.37
Fall 1998	ENEE 350H	*Computer Organization (Honors)*	15	4.92 (of 5)	4.20 (of 5)
	ENEE 698b	*Computer Engineering Seminar*	17		
Spring 1999	ENEE 647	*Design of Distributed Systems*	50	3.58	3.25
	ENEE 499	*Undergraduate Research Project*	3		
	ENEE 499	*Undergraduate Research Project*	1		
Fall 1999	ENEE 350	*Computer Organization*	45	3.73	3.33
Spring 2000	ENEE 759M	*Advanced Topics in Microarchitecture*	18	3.87	3.28
	ENEE 499	*Undergraduate Research Project*	1		
Fall 2000	ENEE 446	*Design of Digital Computers*	27	3.74	3.25
	ENEE 499	*Undergraduate Research Project*	1		
Spring 2001	ENEE 350	*Computer Organization*	20	3.62	3.34
Fall 2001	ENEE 646	*Design of Digital Computers*	70	3.50	3.14
	ENEE 499	*Undergraduate Research Project*	3		
Spring 2002	ENEE 759M	*Advanced Topics in Microarchitecture*	45	3.60	3.20
Fall 2002	ENEE 646	*Digital Computer Design*	66	3.56	3.24
Spring 2003	ENES 100	*Introduction to Engineering Design*	36	3.17	2.99
	ENEE 759H	*High-Speed Memory Systems*	17	3.98	3.23
Fall 2003		**On sabbatical**			
Spring 2004		**On sabbatical**			
Fall 2004	ENEE 302H	*Digital Electronics (Honors)*	24	3.57	3.09
Spring 2005	ENEE 759H	*High-Speed Memory Systems*	12		

Semester	Course No.	Course Title	No. of Students	Teach. Eval. Total Grade	Dept/Coll Avg.
	HONR 218V	*Digital Sound and Fury on Mac OSX: Desktop Publishing, Music, Photography, and Video (University Honors)*	24		
Fall 2005	ENEE 302H	*Digital Electronics (Honors)*	11	3.52	3.29
Spring 2006	ENEE 446	*Design of Digital Computers*	23	3.40	3.34
Fall 2006	ENEE 646	*Design of Digital Computers*	27	3.70	3.30
	ENES 100	*Introduction to Engineering Design*	36		
Spring 2007	ENEE 359A	*Digital VLSI Circuits*	15	3.50	3.16
	ENES 100	*Introduction to Engineering Design*	36		
Fall 2007	ENEE 759H	*High-Speed Memory Systems*	12	3.43	3.11
	ENEE 499	*Undergraduate Research Project*	5		
	ENES 100	*Introduction to Engineering Design*	40	3.50	3.24
Spring 2008	ENEE 359A	*Digital VLSI Circuits*	12	3.82	3.24
	ENEE 159B	*Start-Up 101: Electric Guitar Design*	12	3.65	3.39
	ENES 100	*Introduction to Engineering Design*	40	3.40	3.32
Fall 2008	ENEE 646	*Design of Digital Computers*	21	3.63	3.31
	ENES 100	*Introduction to Engineering Design*	41	3.57	3.10
Spring 2009	ENEE 159B	*Start-Up 101: Electric Guitar Design*	12	3.71	3.29
	ENEE 459J	*Start-Up 101: Consumer Electronics*	12	3.70	3.34
	ENES 100	*Introduction to Engineering Design*	40	3.67	3.25
Fall 2009	ENEE 350H	*Computer Organization (Honors)*	25	3.79	3.24
	ENES 100	*Introduction to Engineering Design*	40	3.55	3.02
	ENEE 359R	*Reverse Engineering (Supervisor)*	11	3.90	3.24
Spring 2010	ENEE 159B	*Start-Up 101: Electric Guitar Design*	12		
	ENES 100	*Introduction to Engineering Design*	40		
	ENEE 499	*Undergraduate Research Project*	3		
	ENEE 499	*Undergraduate Research Project*	1		
Fall 2010		**On sabbatical**			
Spring 2011		**On sabbatical**			

B. Undergraduate Independent Study

ENEE499 Spring 1999	*Full Computer-System Emulation*, with Aamer Jaleel, Jiwanjot Tulsi, and Yun Hua Wang. Design and development of a simulation environment that emulates both a full workstation (including CPU and peripheral IO devices) and a sophisticated operating system (including support for virtual memory, a file system, and multitasking).
ENEE 499 Spring 1999	*Implementing the Ridiculously Simple Computer*, with Julian Requejo. Design and development of a small digital computer from IC components on circuit bread-boards. The computer will be able to run simple applications stored in memory.
ENEE499 Spring 2000	*Development of an Embedded-System Simulation Environment*, with Eric Fiterman. Design and development of an embedded-system simulation environment that emulates the embedded CPU and peripheral IO devices as well as a real-time operating system.
ENEE499 Fall 2000	*A Pipelined Microprocessor on an FPGA*, with Andrew Ripple. Implementation of a high-performance pipelined processor on programmable hardware, including timing specifications and performance measurements.
ENEE 499 Fall 2001	*Verilog Modeling of Real-Time Embedded Systems*, with Vincent Chan, Lei Zong, and David Xia. Development of a Verilog ARM core with support for precise interrupts and programmable I/O controllers.
ENEE 499 Fall 2007	*Analog Circuit Design for Electric Guitars*, with Justin Ahmanson and Timothy Babich. Design and development of a novel preamp and variable EQ circuit for electric guitar, to be used on-board the guitar and powered by 9V battery.
ENEE 499 Fall 2007	*Applications Engineering*, with Garrett Lang, Han Dao, and Jason Borrero. Design and development of web-based application software. One step in the development of a new course to be called *Start-Up 101: Applications Engineering.*
ENEE 499L Summer 2008	*High-Resolution Low-Power A/D Conversion on an Electric Guitar*, with Spencer Black. Development of analog-to-USB and analog-to-firewire DSP units to go on-board an electric guitar.
ENEE499 Spring 2010	*On-Board Low-Power Audio Electronics*, with Rob Brisentine, Noel Cervino, and Matt Wienke. Development of low-power signal-processing electronics to mix synthetic and real-time audio, all run on 9V batteries.
ENEE499 Spring 2010	*A Comparison of Preamps: Transistor-based versus OpAmp-based*, with Ilia Kobrinsky. A comparison of the fidelity and power requirements of two different audio preamp designs.

C. Educational Development

New courses introduced into the regular curriculum

Developed and introduced *ENEE 759M: Advanced Topics in Microarchitecture* (now being taught regularly by two faculty within the Computer Engineering group: Bruce Jacob and Manoj Franklin).

Developed and introduced *ENEE 759H: High-Speed Memory Systems*.

Developed and introduced *ENEE 359A: Digital VLSI Circuits*.

Developed and introduced *ENEE 159B: Electric Guitar Design (Start-Up 101)*.

New courses offered on a trial basis

Developed and introduced several pilot courses that are aimed at educating students on the technical aspects of building real-world artifacts. Due to the confluence of several economic factors, now is an ideal time for students and fresh graduates to start up medium- and high-tech companies on their own. However, most entrepreneurship classes, workshops, and seminars focus on the business aspects of startups (e.g., funding, attracting venture capitalists, writing business plans, etc.), which ignores the technical/design aspects of entrepreneurship. This group of classes is an attempt to bring into the classroom real-world design & development skills—skills that, unlike manufacturing and construction, are *not* being out-sourced.

Start-Up 101: Electric Guitar Design (ENEE 159B). Design and development of circuits in electric guitars, such as analog switches, audio control such as volume and EQ; basic skills and knowledge such as wiring, soldering, electromagnetism, the physics of sound; printed circuit-board design, construction, and assembly. Offered Spring 2008.

Start-Up 101: Consumer Electronics (ENEE 459J). Design and development of hardware/software systems, focusing on issues in real-time operating systems, firmware development, circuit-board design and construction, and correctness of design. Offered Spring 2009.

Start-Up 101: Applications Engineering. Design and development of large, industrial-strength software applications, 10–100 times larger than programs typically developed in the classroom. Offered as ENEE 499 pilot Fall 2007.

Formal course revision & improvement

As Director of Computer Engineering, restructured and reoriented the program's curriculum to address its age and concerns by students, faculty, and graduates that the curriculum needed better structure, cohesiveness, and topical focus. In 2007/8 brought together faculty, current students, and recent graduates to work on the program over numerous focus groups and meetings. The new proposed curriculum strengthened the program's focus on hardware, circuits, and electronics and was informally adopted by the Computer Engineering group via vote in the Fall of 2008. The computer group is working on a formal transition and implementation plan.

Member of a Dean's committee appointed to review and revise *ENES 100—Introduction to Engineering Design*, charged with the task of making the class more attractive to freshmen and more relevant in general. The committee's recommendations resulted in, among other things, the formation by the Dean of *Keystone: The Clark School Academy of Distinguished Professors*, a

cadre of faculty chosen for their proven teaching skills and ability to reach students. ENES 100 is now taught by Keystone professors led by Prof. Bill Fourney (Aero & ME) and has undergone a significant overhaul for the better.

Informal course revision & improvement—ENEE 350:

Revised ENEE 350H to become a project-oriented course, which is very different from the way it had been taught previously, both in content and in instructional delivery. Example informal messages from students in the class expressing their appreciation for the new approach:

> I wanted to take a moment to tell you that I'm really enjoying doing your first project. I've had a small amount of assembler experience before, but I'd never [built] an assembler before, and certainly never had reason to [build] a simulator. Getting these done, and then actually using the tools I'd created to make a working program (the multiply program) was instructive, and simply entertaining.
>
> This is the first time I'd ever essayed an honors course. I'm beginning to wonder what else I've been missing. I'm definitely looking forward to your next project.
>
> —Chuck Robey (350H, F'97)
>
> I just wanted to take a second and thank you for a great semester. This has by far been one of my favorite classes I have ever taken in college. This is a perfect example of how an honors class should be run. Not only did I learn more in this class than all of my other classes combined, but thanks to the many tangents we got off on in class, I was learning about what I was interested in. But most importantly, it was a hell of a lot of fun in the process. There wasn't a single day this semester that I didn't look forward to going to this class, and I must admit that even the countless hours I spent working on the projects was rather enjoyable (I'll probably never say that about homework again). I've done a lot of talking to the other students in the class and I can safely say that everybody else in the class would agree word for word with everything I've said. So keep up the good work and with any luck I'll be in another one of your classes again soon.
>
> —Bruce Knepper (350H, F'97)
>
> I've really enjoyed this course, due mostly to the enthusiasm and insight you bring to lecture, and out of the classroom. You've been very willing to sit down with me and go over questions I had (my stack problems in project 1), and overall it is clear you are dedicated to making time for your students. I really appreciated being able to call you at your office to receive help, and I can't think of many other professors, faculty, etc., who'd be willing to do the same.
>
> The intensity you have brought to lecture has inspired me to focus my under-graduate studies in the area of computer architecture, and you've made it clear how exciting, cutting-edge, and fascinating computer architecture is.
>
> —Eric Fiterman (350H, F'98)
>
> Thank you so much for being a genuinely concerned instructor. I can truthfully say that you brought life to the subject matter in class better than any teacher I have had thus far. We all looked forward to coming to class. The projects were so much fun b/c they were challenging but not confrontational. I loved this about our class. I really hope that we can get a capstone design project together. May I come talk to you about potential research opportunities?
>
> —Jiwanjot (Jyoti) Tulsi (350H, F'98)

This approach was successful in the honors-level course, but it was not clear whether or not it would be successful in the regular version of ENEE 350. The approach was introduced to the regular section in the Fall of 1999 with reactions similar to the following:

> I'd just like to thank you for I must say the most enjoyable class I've had in four years at College Park. I found 350 informative but more importantly captivating. I'm a computer science major, and until this semester thought I was just going to go into the field and make lots of money. Your class makes me want want to throw my job offers away and go to grad school.
>
> —Honter Lin (350, F'99)

The following examples are taken from the ENEE 350 course evaluations (each is from a different evaluation form):

> I know I have a good teacher when my understanding is a function of how much time I put into the class. This is the case here, and since this is now the favorite of my six classes, it gets at least 30% of my attention.
>
> Jacob really does want you to learn and is willing to put in the time and effort to help you do so.
>
> Professor Jacob is by far one of the most effective lecturers I've had at this university. He is always very encouraging of questions and discussion in class, and he consistently illustrates a wealth of knowledge.
>
> This is the kind of course and the kind of professor the University needs more of: people who make the material clear & interesting.

The projects are used by other faculty in the ECE department and CS department as well.

Informal course revision & improvement—ENEE 446/646:

ENEE 446 focuses on the implementation of microprocessors and systems; the class projects were revised to reflect how industrial-strength designs work and how commercial hardware development is done. To begin with, students implement a microprocessor (the "RiSC-16," designed by me) in the Verilog hardware description language; Verilog is a language used in industry that represents hardware in its VLSI implementation, as opposed to a C-language emulation as is used in 350 and was previously used in 446. To this Verilog implementation students add the necessary hardware constructs to allow an operating system to run on the microprocessor: namely, facilities for precise interrupts and virtual memory. Lastly, the students write the rudiments of an operating system, in assembly code, to run on their Verilog microprocessor. A similar approach was introduced in ENEE 646; student feedback was very positive in both undergraduate and graduate offerings:

> I really loved ENEE446 - this is the kind of stuff I always wanted to learn and you made class and the projects fun and interesting.
>
> —Chris Testa (446, S'06)
>
> I would like you to know that I took ENEE 646 with you last Fall (2002) ... you conducted the course in an extremely thorough and professional manner. Your enthusiastic style of teaching in class was mesmerizing (I mean it very seriously) and you handled complex concepts such has Virtual Memory extremely well. The projects were extremely good and they were extremely helpful in understanding the material taught in class. As a result, it gave mea a very good insight into Computer Architecture though that does not happen to be remotely close to my area of research. I would rate your teaching in class easily as one of the best I have ever experienced.
>
> —Amit Mukherjee (646, F'02)

The projects are used by other faculty in the ECE department. Even more interesting is the response from outside the university. For instance, the RiSC-16 architecture is used in places as

far-flung as the University of Illinois at Urbana-Champaign, Université Libre de Bruxelles (Belgium), and Universidad Pontificia Comillas (Spain); the various design documents posted on the class website show up in on-line databases as cited works; numerous developers have contacted me over the years to help them build VLSI implementations of the processor design (google "RiSC-16 maryland" for examples); and the implementation of precise interrupts, an extremely important mechanism that had previously been neglected in *all* computer-systems textbooks—despite the fact that it is nearly impossible to build a working microprocessor without precise interrupts—began to show up in undergraduate texts several years after the RiSC-16 design documents were first posted.

D. Advising (research)

Currently Supported Graduate Students:

Ishwar Bhati (Ph.D.)

Mu-Tien Chang (Ph.D.)

Elliott Cooper-Balis (Ph.D.)

Eric Nietering (M.S.)

Paul Rosenfeld (Ph.D.)

Jim Stevens (Ph.D.)

Paul Tschirhart (Ph.D.)

Graduated Ph.D. Students:

Cagdas Dirik, Ph.D. 2009. *Performance and Analysis of NAND Flash Memory Solid-State Disks*. (SanDisk)

Sadagopan Srinivasan, Ph.D. 2007. *Prefetching vs. the Memory System: Optimizations for Multi-core Server Platforms*. (Intel)

Brinda Ganesh, Ph.D. 2007. *Understanding and Optimizing High-Speed Serial Memory-System Protocols*. (Intel)

Ankush Varma, Ph.D. 2007. *High-Speed Performance, Power, and Thermal Co-Simulation for SoC Design*. (Intel)

Nuengwong (Ohm) Tuaycharoen, Ph.D. 2006. *Disk Design-Space Exploration in Terms of System-Level Performance, Power, and Energy Consumption*. (Dhurakijpundit University, Thailand)

Samuel Rodriguez, Ph.D. 2006. *myCACTI: A New Cache-Design Tool for Pipelined Nanometer Caches*. (AMD)

Aamer Jaleel, Ph.D. 2005. *The Effects of Out-of-Order Execution on the Memory System*. (Intel)

David Tawei Wang, Ph.D. 2005. *Modern DRAM Memory Systems: Performance Analysis and a High Performance, Power-Constrained DRAM-Scheduling Algorithm*. (MetaRAM, a Silicon Valley start-up)

Brian Davis, Ph.D. 2000. *Modern DRAM Architectures*. Davis was a doctoral student at the University of Michigan; I was his thesis co-chair with Trevor Mudge. (Michigan Technological University)

Graduated M.S. Students:
(only MS with theses listed)

Jeffrey Scott Smith, M.S. 2006. *Distributed Two-Dimensional Fourier Transforms on DSPs with Applications for Phase Retrieval*. (NASA)

Rami Nasr, M.S. 2005. *FBsim and the Fully Buffered DIMM Memory System Architecture*. (Lutron)

Amol Gole, M.S. 2003. *TERPS: The Embedded Reliable Processing System*. (U.S. Patent Office)

Bharath Iyer, M.S. 2003. *Extended Split-Issue Mechanism in VLIW DSPs to Support SMT and Hardware-ISA Decoupling*. (AMD)

Nuengwong Tuaycharoen, M.S. 2003. *RTOS-Based Dynamic Voltage Scaling*. (continuing as U. Maryland Ph.D. student)

Lei Zong, M.S. 2003. *Nanoprocessors: Configurable Hardware Accelerators for Embedded Systems*. (Army Research Lab)

Brinda Ganesh, M.S. 2002. *Architectural Support for Embedded Operating Systems*. (continuing as U. Maryland Ph.D. student)

Aamer Jaleel, M.S. 2002. *In-Line Interrupt Handling and Lockup-Free TLBs*. (continuing as U. Maryland Ph.D. student)

Paul Kohout, M.S. 2002. *Hardware Support for Real-Time Operating Systems*. (EVI Technology)

Tiebing Zhang, M.S. 2001. *RTOS Performance and Energy Consumption Analysis Based on an Embedded System Testbed*. (Aeptec Microsystems)

Christopher Collins, M.S. 2000. *Emulation of Embedded Microcontrollers and Real-Time Operating Systems*. (Intel)

Undergraduate Research:

Kathleen Baynes (as part of the MERIT/ICE program, Summer 2000): *Power Modeling of Embedded Systems*

Spencer Black (as part of ENEE 499L, Summer 2008): *High-Resolution Low-Power A/D Conversion on an Electric Guitar*.

Vincent Chan (as part of ENEE 499, Fall 2001): *Verilog Modeling of Real-Time Embedded Systems*

Brian Davis (as part of the MERIT/ICE program, Summer 2002): *Direct-DRAM-to-DRAM - Access to Support High-Level Data Movement*

Eric Fiterman (Summer 1999): *Microarchitecture-Level Emulation of Real-Time Embedded Systems*

Benjamin Garrett (Fall 1998): *A Speculative Architecture for Handling Precise Interrupts*

Benjamin Garrett (as part of ENEE 759M, Spring 1998): *Miss Handling in Software-Managed TLBs*

Kevin Ghozati (Summer 2002): *Nanoprocessor Modeling for Real-Time Embedded Systems*

Aamer Jaleel (as part of ENEE 499, Spring 1999): *Design of a Provably Correct Operating System*

Aamer Jaleel (1999–2000): *A Performance Study of Several Virtual Memory Mechanisms*

Sandy Klemm (as part of the MERIT/ICE program, Summer 2002): *Applying Control Theory to Dynamic Voltage Scaling*

Jeremy Monaldo (Spring/Summer 2002): *Nanoprocessor Modeling for Real-Time Embedded Systems*

Joe Nuzman (as part of ENEE 759M, Spring 1998): *A Simulation of Explicit Multi-Threading*

Daniel O'Brien (as part of the MERIT/ICE program, Summer 2001): *High-Performance Benchmarks for Real-Time Embedded Systems*

Ken Powers (Summer 1999): *A Study of DRAM Architectures and Organizations*

Paul Rosenfeld (Summer 2007): *Modeling High-Performance DRAM Systems*

James Shen (Summer 2007): *Embedded Wireless Networks*

Christine Smit (as part of the MERIT/ICE program, Summer 2000): *Power Modeling of Embedded Systems*

Jiwanjot Tulsi (as part of ENEE 499, Spring 1999): *Design of a Provably Correct Operating System*

Yun Hua Wang (as part of ENEE 499, Spring 1999): *Design of a Provably Correct Operating System*

David Xia (as part of ENEE 499, Fall 2001): *Verilog Modeling of Real-Time Embedded Systems*

Lei Zong (as part of the MERIT/ICE program, Summer 2001): *High-Performance Benchmarks for Real-Time Embedded Systems*

Lei Zong (as part of ENEE 499, Fall 2001): *Verilog Modeling of Real-Time Embedded Systems*

High-School Student Research:

Ben Li (high-school research internship for the Magnet Program at Montgomery Blair High School, Summer 2006): *Performance Modeling of Advanced DRAM Systems*

Andrea Ng (high-school research internship for the Magnet Program at Montgomery Blair High School, Summer 2009): *Hardware Validation of Simulators*

Colin Schmidt (high-school research internship for the Magnet Program at Montgomery Blair High School, Summer 2008): *Validating a DRAM-System Simulator*

Advising (non-research)

Inventis Mentoring. The Inventis mentoring program spans the Engineering College; the mentors are selected by the program organizers. Have advised roughly a dozen students in this program since its inception in 2004.

Undergraduate ECE Mentoring. The ECE department has a formal advising/mentoring program in which students are assigned to faculty; students cannot register for classes without meeting with their faculty advisor. Currently advise roughly fifteen ECE undergraduates.

Education-Related Honors and Awards:

Invited to speak at the *National Student Leadership Conference*, a week-long seminar for high-school students who have shown academic talent. Summer 2008, and again Summer 2009.

Clark School of Engineering Keystone Professor. One of six professors named to Keystone: The Clark School Academy of Distinguished Professors, 2006.

Award for Teaching Excellence, University of Maryland (campus-wide). In recognition of excellence in teaching at the undergraduate level, May 2004.

In February, 2003, The Computer Engineering Handbook (a title to which I contributed the following chapter) was honored as an Outstanding Academic Title for 2002 by *Choice Magazine*, a publication of the American Library Association.

B. Jacob. "Virtual Memory Systems and TLB Structures." In The Computer Engineering Handbook, pp. 5:55–5:65. V. Oklobdzija, Editor. CRC Press: Boca Raton FL, 2002.

Selections for this honor are made based upon "their excellence in scholarship and presentation, the significance of their contribution to the field, and their value as important—often the first—treatment of their subject."

General Co-Chair for 5th Workshop on Computer Architecture Education, January 1999.

George Corcoran Memorial Award, 1998/9 academic year. "In recognition of teaching and educational leadership at the University of Maryland, College Park campus, effective contribution at the national level, and creative and other scholarly activities related to Electrical and Computer Engineering education."

IV. SERVICE

A. Professional Service

Editorial Service

Associate Editor, *IEEE Computer Architecture Letters*, 2007–2011.

Associate Editor, *ACM Transactions on Embedded Computing Systems (TECS)*, 2006–2009.

Co-Editor, Special Inaugural Issue of *ACM Transactions on Embedded Computing Systems (TECS)*, vol. 1, no. 1, December 2002.

Proposal-Review Panels

Panelist, National Science Foundation, March 2008.

Panelist, National Science Foundation, October 2003.

Panelist, National Science Foundation, November 2003.

Panelist, National Science Foundation, February 2002.

Organizing Committees

Panel Discussion Coordinator: *Memory Systems—What's the Real Problem? What's the Next Solution?* Held at the Workshop on Memory System Performance and Correctness (MSPC 2008), March 2008.

Session Chair, 13th International Symposium on High-Performance Computer Architecture (HPCA 2007), February 2007.

Session Chair, International Symposium on Low Power Electronics and Design (ISLPED 2006), October 2006.

Workshops Chair, 8th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2005), September 2005.

Local Arrangements Chair, 7th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2004), November 2004.

Coordination Vice-Chair, 5th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2002), November 2002.

Publicity Chair, 2nd Workshop on Compiler and Architecture Support for Embedded Systems (CASES 1999), October 1999.

General Co-Chair, 5th Workshop on Computer Architecture Education (WCAE'99), January 1999.

Local Arrangements Chair, 3rd IEEE Symposium on High-Assurance Systems Engineering (HASE 1998), November 1998.

Program Committees

Board of Distinguished Reviewers, International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC), January 2012.

Program Committee Member, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2011), October 2011.

Program Committee Member, 43rd International Symposium on Microarchitecture (MICRO 2010), December 2010.

Program Committee Member, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2010), October 2010.

Program Committee Member, 41st International Symposium on Microarchitecture (MICRO 2008), November 2008.

Program Committee Member, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2008), November 2008.

Program Committee Member, International Conference on Computer Design (ICCD 2008), October 2008.

Program Committee Member, Workshop on Memory System Performance and Correctness (MSPC 2008), March 2008.

Program Committee Member, 13th International Symposium on High-Performance Computer Architecture (HPCA 2007), February 2007.

Program Committee Member, 39th International Symposium on Microarchitecture (MICRO 2006), December 2006.

Program Committee Member, 9th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2006), October 2006.

Program Committee Member, International Conference on Computer Design (ICCD 2006), October 2006.

Program Committee Member, 8th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2005), September 2005.

Program Committee Member, 2005 Memory Systems Performance Workshop (MSP 2005), June 2005.

Program Committee Member, 7th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2004), November 2004.

Program Committee Member, 6th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2003), November 2003.

Program Committee Member, 4th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2001), November 2001.

Program Committee Member, Workshop on Memory Performance Issues, June 2001.

Program Committee Member, 4th IEEE Symposium on High-Assurance Systems Engineering (HASE 1999), November 1999.

General Reviewing

Reviewer for papers in the following journals:

IEEE Transactions on Computers
IEEE Transactions on Parallel and Distributed Systems
IEEE Transactions on Very Large Scale Integration Systems
IEEE Computer
ACM Transactions on Embedded Computing Systems
ACM Transactions on Architecture and Code Optimization
ACM Computing Surveys
IBM Journal of Research and Development
The Computer Journal

Reviewer for papers in the following annual meetings:

ACM/IEEE International Symposium on Computer Architecture (ISCA)
ACM/IEEE International Symposium on Microarchitecture (MICRO)
ACM International Conference on Supercomputing (ICS)
IEEE International Symposium on High-Performance Computer Architecture (HPCA)
IEEE International Symposium on High-Assurance Systems Engineering (HASE)
IEEE International Conference on Computer Design (ICCD)
Int'l Conf. on Compilers, Architectures, and Synthesis for Embedded Systems (CASES)
Workshop on Computer Architecture Education (WCAE)

B. University Service

Departmental

2007–2010	Director, Computer Engineering Program
2006–2011	Member, ECE PhD Qualifying Exam Committee
2006–2007	Prepared accreditation materials for Middle States Commission on Higher Education
2005–2007	Member, ECE Faulty Search Committee
2005–2006	Prepared materials for ABET accreditation process
Spring 2005	ECE search committee for *Chairperson of the ECE Department*
2004–2007	Member, ECE Promotion and Tenure Committee
Spring 2004	ECE search committee for *Director of Computing Facilities* position
2002–2004	Member, ECE Department Council
Spring 2001	ECE search committee for *Chairperson of the ECE Department*
2000–2002	Member, ECE Facilities and Services Committee
1999–2000	Member, ECE Undergraduate Affairs Committee
1998–1999	Chair, ECE Undergraduate Affairs Committee
1998–2000	Organized the weekly *Research in Computer Engineering Colloquium*. During this period, we had a talk every week (during the academic year).
1998–2000	Member, ECE General Academic Affairs Committee

1998– Member, ECE Curriculum Revision Committee

1998–2000 Computer Engineering representative for ABET transition

Spring 1998 ECE search committee for Personnel and *Research Coordinator* position

Spring 1998 ECE search committee for *Systems Analyst* position

1997–1998 Organized a weekly Microarchitecture Seminar Series

College

2005–2008 Member, Engineering College Promotion and Tenure Committee

2004–2005 Member, Dean's committee formed to review and revise *ENES 100—Introduction to Engineering Design*

1999–2001 Member, ECE College of Engineering Council

University

2010 Accepted nomination for membership on the University of Maryland Athletic Council (University Senate will vote May 5th)

2006–2007 ECE representative/member of CS Department Curriculum Review Committee

1999–2003 Faculty advisor for university chapter of Eta Kappa Nu (EE Honor Society)

➡ The Maryland chapter received the Certificate of Merit from the national Eta Kappa Nu Association for Outstanding Chapter Activities, 1999–2000 academic year. The two other chapters receiving the same award were from Carnegie Mellon and MIT.

C. Community Service

Fall 2001 *Pro bono* technical consulting for lawyers representing the US Department of Justice on the Microsoft antitrust case

Spring 2010 Spoke to high-school seniors for Career Day at Baltimore Polytechnic Institute, a Blue Ribbon School of Excellence in Baltimore, MD